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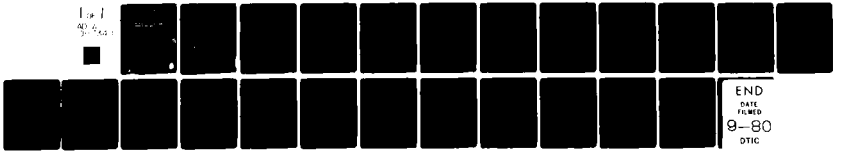

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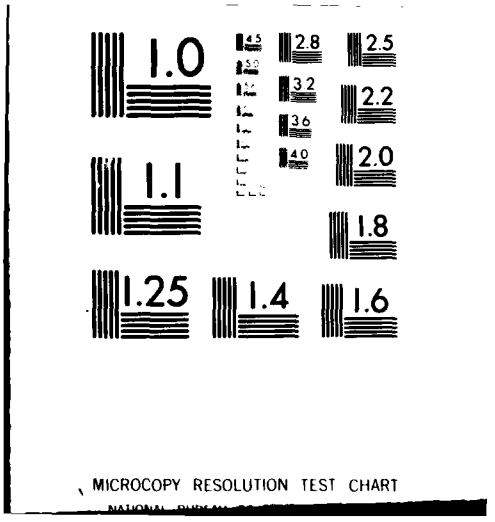
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Report SAM-TR-80-1

LEVEL II

USAFSAM WAIVER FILE INTELLIGENT TERMINAL: HARDWARE REFERENCE MANUAL

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April 1980

Final Report for Period October 1976 - June 1979

Approved for public release; distribution unlimited.

USAF SCHOOL OF AEROSPACE MEDICINE
Aerospace Medical Division (AFSC)
Brooks Air Force Base, Texas 78235

NOTICES

This final report was submitted by personnel of the Aeromedical Cybernetic Branch, Clinical Sciences Division, USAF School of Aerospace Medicine, Aerospace Medical Division, AFSC, Brooks Air Force Base, Texas, under job order 7755-20-09.

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This report has been reviewed by the Office of Public Affairs (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The hardware design and configuration of an intelligent microcomputer terminal is described. This terminal is used to access a data base on a larger main-frame computer. The system was designed to provide maximum flexibility at the users fingertips by making the complex data-base management system (DBMS) of the main-frame computer transparent to the user. All aspects of the system configuration are outlined to provide sufficient knowledge for maintenance and repair.

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USAFSAM WAIVER FILE INTELLIGENT TERMINAL: HARDWARE REFERENCE MANUAL

INTRODUCTION

This manual describes the most pertinent hardware-design aspects of the USAFSAM Waiver File Intelligent Terminal. The operation of peripheral devices is not described, but a detailed reference-manual list is provided. Our primary intent has been to adequately document all hardware design features so that the system might be properly maintained. This manual consists of:

- Main-Frame Hardware Description--covering the overall hardware-system configuration of the Waiver File Intelligent Terminal and describing the complete AC power distribution.

- Peripheral Input/Output Interfaces--covering all modifications needed to implement the various peripheral devices; also outlining wire-wrap changes, solder changes, and integrated circuit driver/terminator requirements.

- Software Control Information--providing the necessary link to the hardware/software boundary concerning programming of intelligent large-scale integrated (LSI) circuit devices.

- Hardware Reference Manual List

- System Cable Diagrams

MAIN-FRAME HARDWARE DESCRIPTION

The USAFSAM Waiver File Intelligent Terminal (Fig. 1) is a hybrid of many state-of-the-art microprocessor-based systems. The foundation consists of an Intel SBC 660 chassis main frame that includes:

1. SBC 80/20 single-board computer for the central processing unit (CPU)

2. SBC 104 general purpose input/output (I/O) and memory board

3. SBC 108 general purpose input/output (I/O) and memory board

4. two SBC 016 16K memory boards

The combination of the five boards provides a total main-frame capability as described below:

CPU	Intel 8080A-2 microprocessor
Memory	46-K-byte dynamic random access memory (RAM) 12-K-byte erasable programmable read-only memory (EPROM)

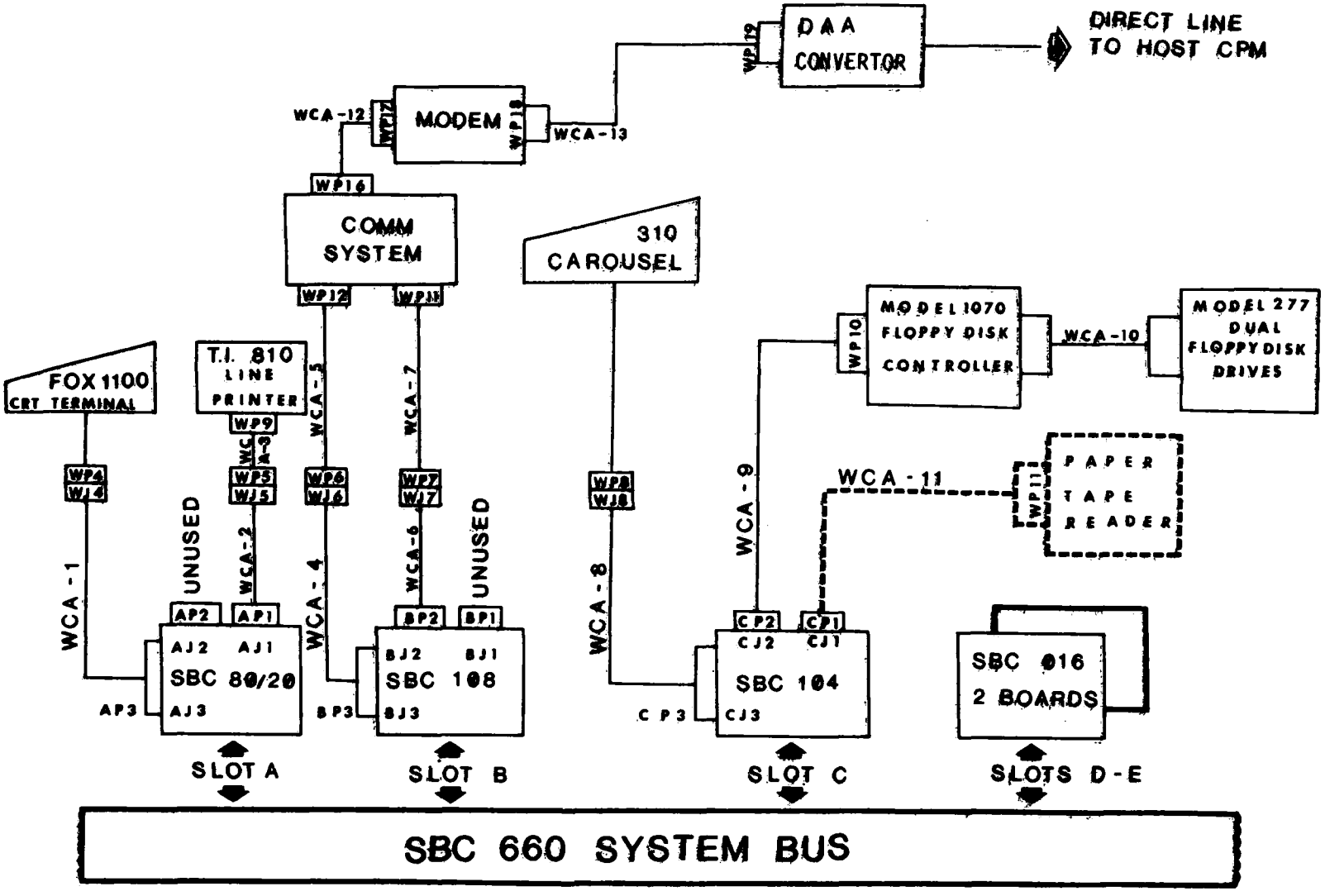

Figure 1. Waiver File Intelligent Terminal system configuration.

I/O	3 RS-232C serial ports 18 (8-bit) parallel ports
Clock	2.15 MHz

The entire system memory has been sectioned for dedicated devices and user space (Fig. 2).

The microcomputer main frame interfaces to a host of peripheral devices:

1. The PerSci Dual Floppy Disk System consists of a Model 277 dual drive and a Model 1070 intelligent controller. This is a single-sided single-density floppy-disk system which utilizes the IBM 3740 format. All mass storage for the Waiver File system is handled by the floppy disk which provides a 0.5-megabyte memory-storage capability. The other peripheral devices are operator-oriented character I/O.

2. The operator's console is a Fox 1100 CRT serial-data terminal which operates at 9600 baud. All commands for the system are normally processed through this terminal; however, the console can be assigned to the Carousel 310 terminal. This is a 300-baud communications device that can provide letter-quality data output as required. The combination of the two terminals provides the operator maximum flexibility in communicating with the system.

3. A Texas Instruments (T.I.) Model 810 printer provides relatively high-speed character output, operating at speeds up to 160 characters per second. This is a matrix impact printer and can be used for most Waiver File reports.

4. A communication-system interface (WJ6 & WJ7, Fig. 1) was designed to operate with an encryption/decryption device (comm system, Fig. 1). When long-distance communications with the host computer were required, the comm system could be used to insure data integrity. Operation of the Waiver File Intelligent Terminal in this mode required a modem and special DAA convertor. Due to changed location of the Waiver File Intelligent Terminal, the comm system as designed is no longer planned for use; only the serial-communications port (available through connector WJ6) will be used.

5. A high-speed paper-tape reader (Fig. 1) is available for laboratory testing. This capability is used only within the design laboratory and is not supported for the operational terminal.

For maintenance purposes, a back-panel layout has been included (Fig. 3) to show the board configuration in the main-frame chassis, as well as the appropriate connector terminations.

The AC distribution system provides maximum simplicity in the power-up procedure. A keylock switch on the front panel allows all secondary systems to be powered up at one time. As shown in Figure 4, switch KS turns on an indicator lamp (LI) and a cooling fan and applies power to RLY1, which in turn switches on an AC distribution panel.

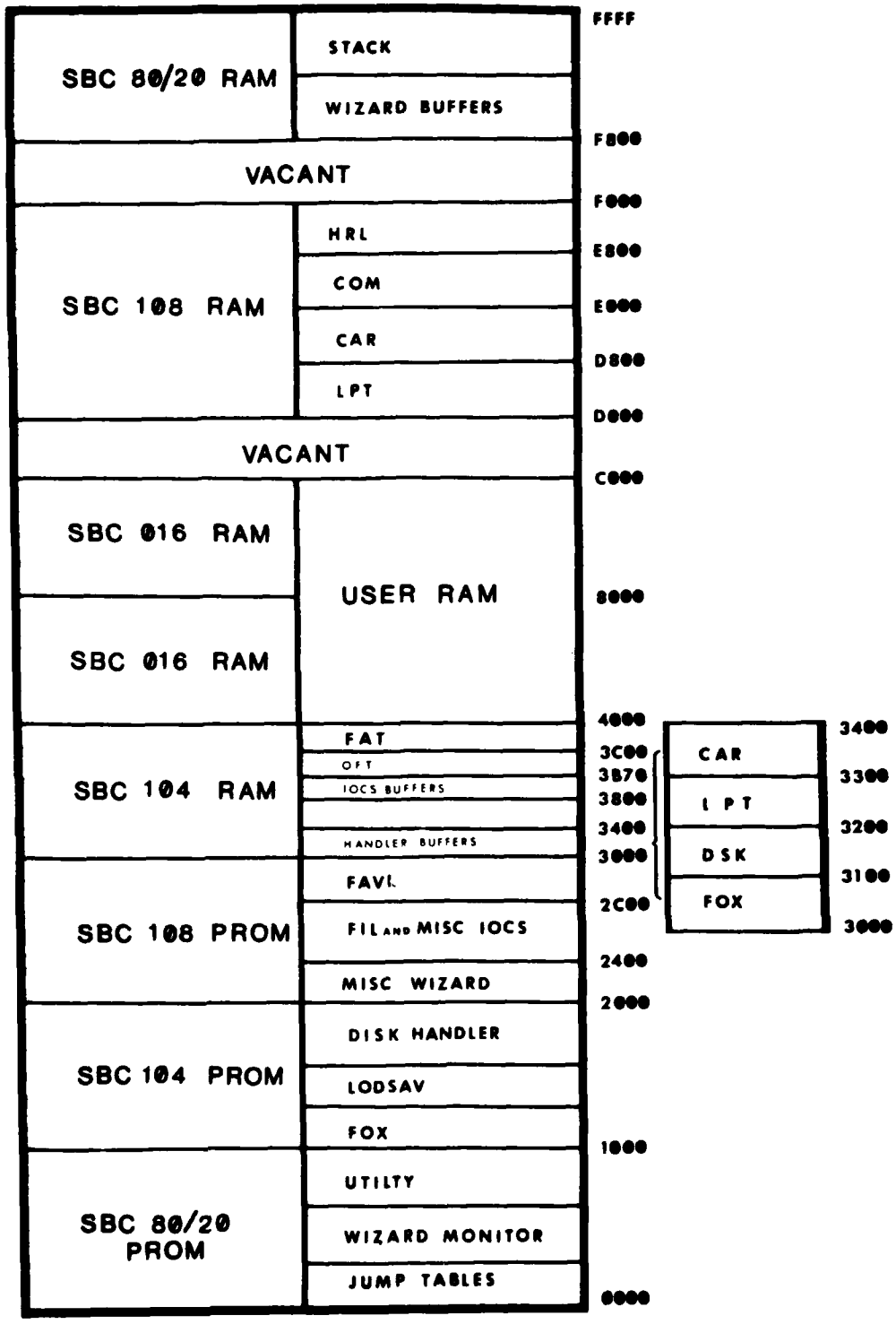

Figure 2. Waiver File WIZARD memory map.

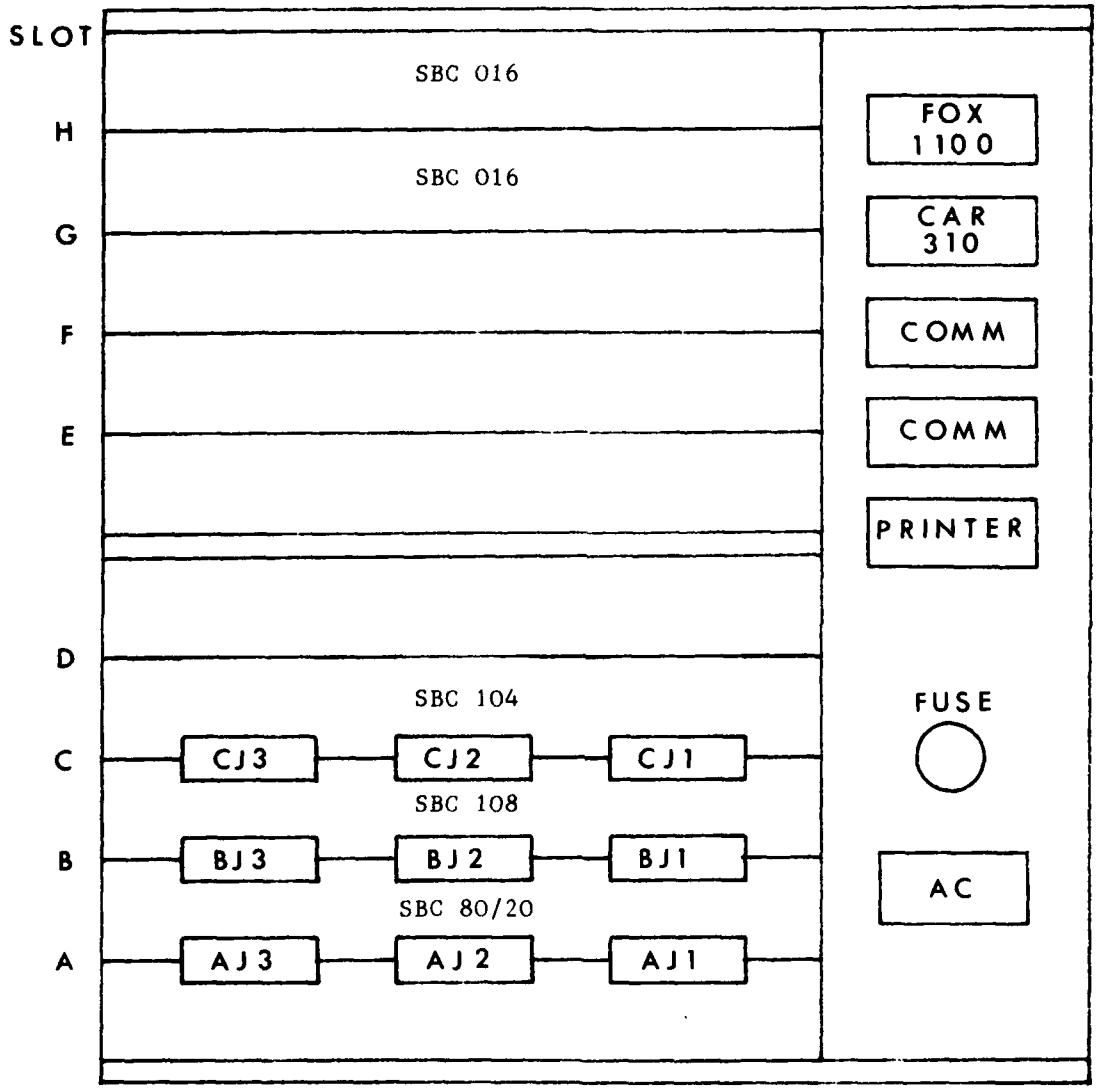

Figure 3. Waiver File back panel layout.

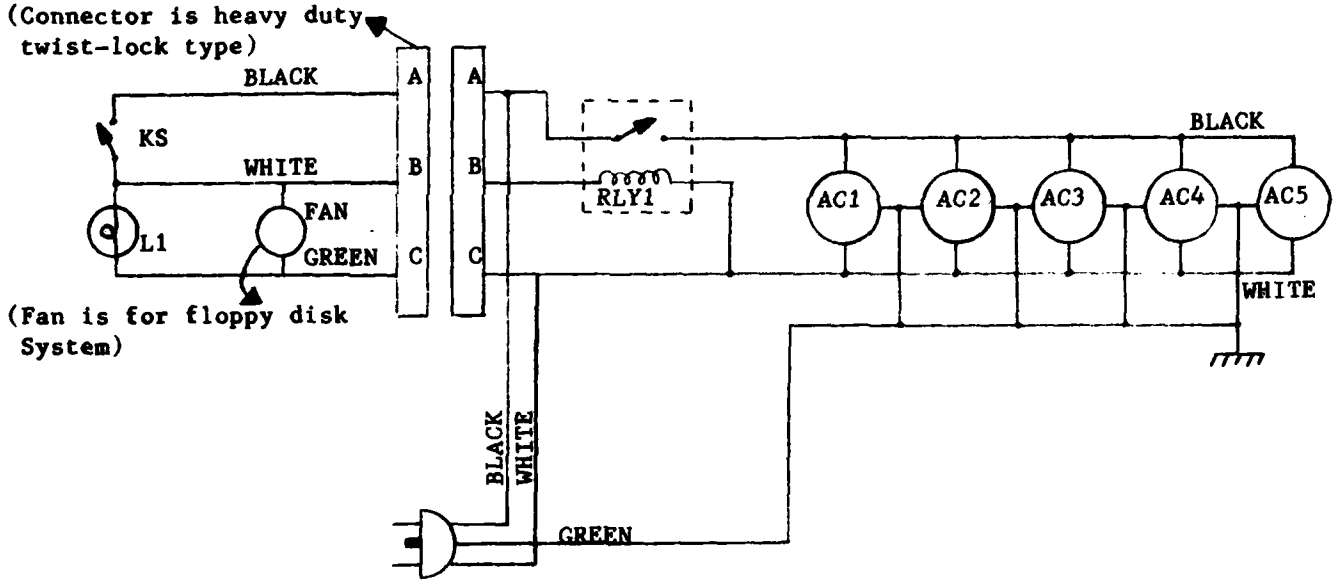

Figure 4. Waiver File AC power distribution.

PERIPHERAL INPUT/OUTPUT INTERFACES

Within the Waiver File Intelligent Terminal system, three boards (the SBC 80/20, 104, and 108) have input/output interfaces with various peripheral devices. The I/O address port assignments for the entire Waiver File system are shown in Table 1. This table should be referred to when new I/O devices are added to the system. Any changes should be immediately noted in the table to preserve system integrity.

TABLE 1. WAIVER FILE I/O ADDRESS SYSTEM

Address	Board	Assignment
00H-AFH		Unused
B0H	SBC 104	Interrupt mask status (read only)
B1H	"	Read/Write interrupt mask
B2H	"	Reset 1-msec interval timer (write only)
B3H	"	Combination to accomplish same as at B1H & B2H
B4H	"	Group 1, Port A, unused
B5H	"	Group 1, Port B, paper-tape-reader data out
B6H	"	Group 1, Port C, paper-tape-reader control
B7H	"	Group 1, Command address
B8H	"	Group 2, Port A, floppy-disk data I/O
B9H	"	Group 2, Port B, floppy-disk control
BAH	"	Group 2, Port C, floppy-disk control
BBH	"	Group 2, Command address
BCH	"	Carousel 310, serial-data I/O
BDH	"	Carousel 310, serial-port Command address
BEH	"	Same as BCH
BFH	"	Same as BDH
C0H	SBC 108	Interrupt mask status (read only)
C1H	"	Read/Write interrupt mask
C2H	"	Reset 1-msec interval timer (write only)
C3H	"	Combination to accomplish C1H & C2H
C4H	"	Group 3, Port A, unused
C5H	"	Group 3, Port B, unused
C6H	"	Group 3, Port C, unused
C7H	"	Group 3, Command address, unused
C8H	"	Group 4, Port A, unused
C9H	"	Group 4, Port B, comm system control
CAH	"	Group 4, Port C, comm system control
CBH	"	Group 4, Command address
CCH	"	Comm system, serial-data I/O
CDH	"	Comm system, serial-port Command address
CEH	"	Same as CCH
CFH	"	Same as CDH
D0H	N/A	Not used
D1H	N/A	Not used
D2H	N/A	Not used
D3H	N/A	Not used

TABLE 1. (Cont)

D4H	SBC 80/20	Power fail status/latch
D5H	"	System bus override
D6H	"	LED diagnostic indicator
D7H	"	Not used (not available)
D8H	"	Intel 8259 Interrupt controller (read/write)
D9H	"	Intel 8259 Interrupt controller (read/write)
DAH	"	Same as D8H
DBH	"	Same as D9H
DCH	"	Intel 8253 Interval timer, read/load cntr 0, unused
DDH	"	Intel 8253 Interval timer, read/load cntr 1 (real-time Clk)
DEH	"	Intel 8253 Interval timer, read/load cntr 2 (baud rate)
DFH	"	Intel 8253 Interval timer, load mode control
E0H	N/A	Not used
E1H	N/A	Not used
E2H	N/A	Not used
E3H	N/A	Not used
E4H	SBC 80/20	Group 5, Port A, T.I. 810 control
E5H	"	Group 5, Port B, T.I. data out
E6H	"	Group 5, Port C, T.I. control
E7H	"	Group 5, Command address
E8H	"	Group 6, Port A, unused
E9H	"	Group 6, Port B, unused
EAH	"	Group 6, Port C, unused
EBH	"	Group 6, Command address
ECH	"	Intel 8251 USART, Console data I/O
EDH	"	Intel 8251 USART, Command address

The SBC 80/20 provides the I/O capability for the Fox 1100 console as well as output to the T.I. 810 line printer. The Fox 1100 communicates via a standard RS-232C serial interface, whereas the line printer is configured for centronics compatible parallel operation. Cable diagrams for these interfaces can be found in Appendix B, Figure B-1.

All standard microcomputer boards used in the Waiver File system require specific wire-wrap modifications for proper use. The SBC 80/20 changes are outlined in Table 2. The SBC 80/20 hardware reference manual should be referred to when questions arise concerning the function of any specific wire-wrap change. Certain driver/terminator chips, listed in Table 2, have been installed to provide the needed interface voltage levels.

The SBC 104 and 108 board modifications are listed in Tables 3 and 4 respectively. The SBC 104/108/116 hardware reference manual should be referred to concerning any wire-wrap changes made, as well as driver/terminator installations.

TABLE 2. SBC 80/20 (SLOT A) WIRE-WRAP MODIFICATIONS*

Function	Delete	Add
Select A1 & A2 direction	52-53	51-52
Cntr 1 to IR0 (real-time clock)		24-34
INT1 to IR1 (comm sys. RXR & TXR)	25-45	25-44
RXR to IR2 (console CRT)	26-35	26-41
TXR to IR3 (console CRT)		27-40
PIB1 to IR4 (line printer)		28-69
INT5 to IR5 (carousel RXR & TXR)		29-48
IR7 (no interrupt)		36-37-38-39-31

Driver/Terminator Requirements

Socket	Driver/Terminator
A3	SN 7437
A4	SBC 901
A5	SN 7437
A6	SN 7437

*All pins not listed remain in default configuration.

TABLE 3. SBC 104 (SLOT C) WIRE-WRAP MODIFICATIONS*

Function	Delete	Add
I/O address select (switch S2)	1-4	1-6
RXR & TXR to INT5	103-111	96-97-107
A7 & A8 direction select	65-66,52-53	53-56
Mode 2 STB line	63-64	62-64
Mode 2 ACK line	57-58,67-68	58-68
READ for floppy disk		61-62
Data set ready	15-16	16-17
Data terminal ready	17-18	15-18
Request to send	21-22	20-21
Clear to send		19-20
Baud-rate select (switch S1)	1-4	1-7
Convert READ to READ (this wire is soldered)	59-60	A9-8 to A9-12

Driver/Terminator Requirements

Socket	Driver/Terminator
A3	SN 7437
A4	SBC 902
A5	SBC 902
A6	SBC 902
A9	SN 7437
A11	SN 7437
A12	SN 7437

*All pins not listed remain in the default configuration.

TABLE 4. SBC 108 (SLOT B) WIRE-WRAP MODIFICATIONS*

Function	Delete	Add
RXR & TXR to INT1	103-111	96-97-111
Baud-rate select (switch S1)	1-4	1-7
I/O address select (switch S2)	1-4	1-5
RAM-base address select	89-90	90-91
Request to send		
Clear to send	19-20	19-21

Driver/Terminator Requirements

Socket	Driver/Terminator
A9	SN 7437
A10	SN 7437
A11	SBC 901

Special Modifications**

Function	Delete	Add
Protocol select (bit 0)	63-64	63-61
Protocol select (bit 1)	65-66	65-63
Protocol select (bit 2)	67-68	67-65
Baud-rate select (bit 4)	61-62	61-59
Baud-rate select (bit 5)	59-60	59-54

*All pins not listed remain in the default configuration.

**This wire-wrap configuration sets the proper bit pattern for protocol 0 and 1200 baud to the comm box. This has been done to prevent a race condition between the comm box and the Waiver File Intelligent Terminal.

The major peripheral devices were defined in the Main-Frame Hardware Description section. The floppy-disk system, however, is not a stand-alone peripheral device, as are the others, and its unique I/O interface warrants further discussion. The Model 277 PerSci floppy disk communicates to the Waiver File system through the Model 1070 intelligent controller. A parallel, rather than serial, communications interface has been implemented to ensure maximum communications speed. The PerSci user's manual for the intelligent diskette controller should be referred to for questions regarding specifics of the parallel interface. Basically, the interface consists of a bidirectional 8-bit data bus along with 5 control lines for selecting read, write, status, data, and reset conditions. Power for the controller is derived from the SBC 660 chassis power supply, as indicated in Figure 5.

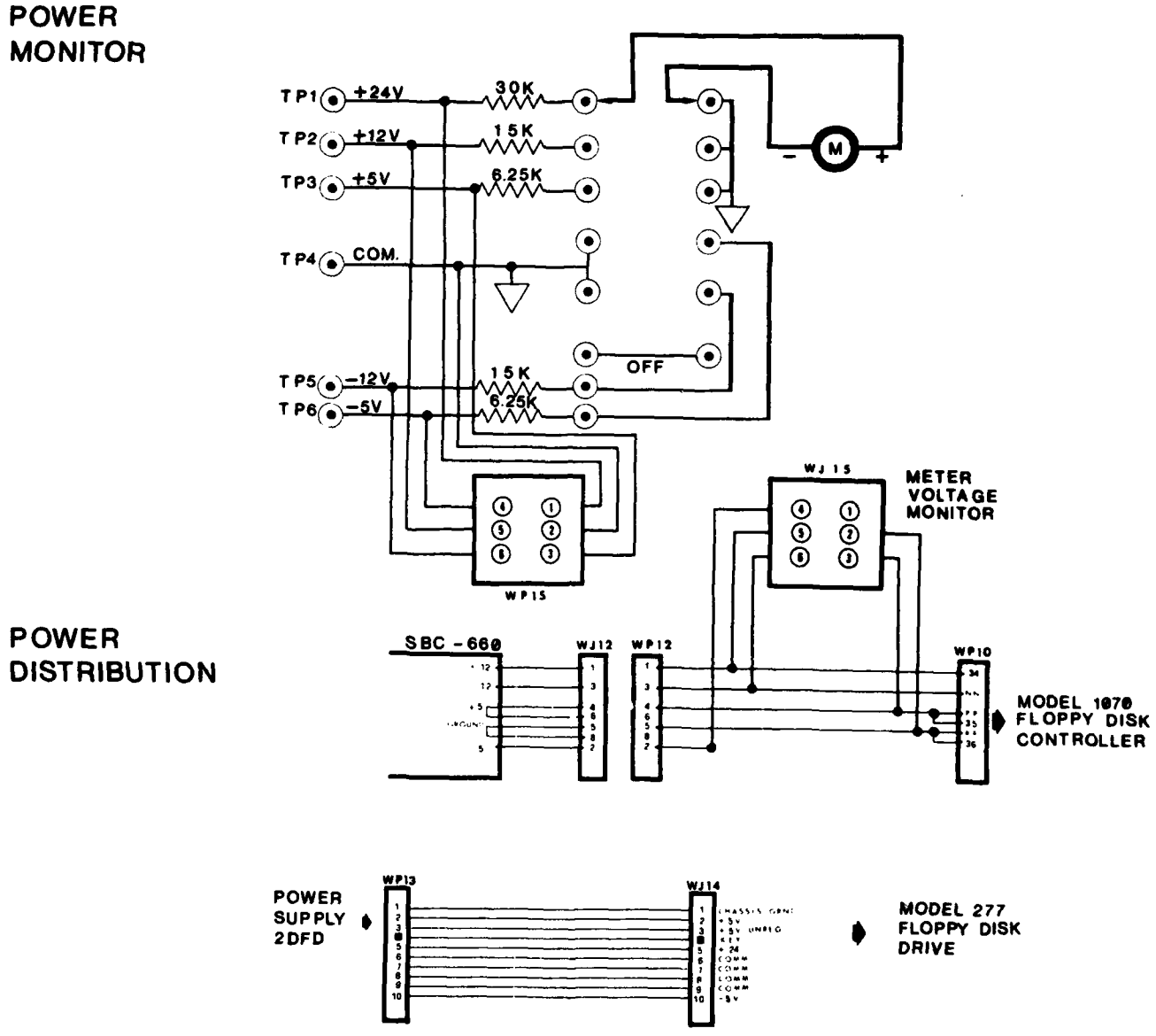

Figure 5. Floppy-disk/meter circuit.

SOFTWARE CONTROL INFORMATION

Before communication with peripheral devices is possible, programmable peripheral-interface chips must be initialized. The modes assigned to all parallel-communications chips (Intel 8255) are outlined in Table 5. Because

TABLE 5. INTEL 8255 PROGRAMMABLE PERIPHERAL INTERFACE I/O ADDRESSES AND PROGRAMMED MODES

SBC 104		Mode Description
Group 1:	CMDAD1 = 0B7H PORT1A = 0B4H PORT1B = 0B5H PORT1C = 0B6H GP1MOD = 081H	Programmed in Mode 0 with Port B as data output and Port C as control. Port A is unused.
Group 2:	CMDAD2 = 0BBH PORT2A = 0B8H PORT2B = 0B9H PORT2C = 0BAH CP2MOD = 0F8H	Programmed in Mode 2 with Ports A & C providing bidirectional communication. Port B is programmed in Mode 0 for output control. Entire group is used for floppy disc.
SBC 108		
Group 3:	CMDAD3 = 0C7H PORT3A = 0C4H PORT3B = 0C5H PORT3C = 0C6H GP3MOD = ----	Unused at present time.
Group 4:	CMDAD4 = 0C8H PORT4A = 0C8H PORT4B = 0C9H PORT4C = 0C9H GP4MOD = ----	Unused at present time.
SBC 80/20		
Group 5:	CMDAD5 = 0E7H PORT5A = 0E4H PORT5B = 0E5H PORT5C = 0E6H GP5MOD = 094H	Programmed with Ports B & C in Mode 1, with Port A in Mode 0 as input. Port C Hi bits are in output mode.
Group 6:	CMDAD6 = 0EBH PORT6A = 0E8H PORT6B = 0E9H PORT6C = 0EAH GPGMOD = ----	Unused at present time.

of the common standard-device nomenclature, each programmable port and mode word has been uniquely identified. Note that Table 5 identifies six groups of parallel ports; two on each microcomputer board. Each group has three ports, labeled A, B, and C; therefore, PORT 1A refers to group 1 port A. This labeling scheme is used throughout the Waiver File system. Also, each group has a command address and a mode word: these are labeled CMDAD1 and GP1MOD for the group 1 ports. The only part that changes for other groups is the group reference number. The actual modes are included in Table 5 for easy reference and are thoroughly explained in the SBC 80/20 hardware reference manual.

The interrupt structure planned for the Waiver File system is shown in Table 6. Existing wire-wraps on all boards have been configured for this structure; however, the required software has not been implemented to accommodate these interrupts. Any conversion of this system to the interrupt-driven mode must be done very carefully since the software device handlers would require considerable modification.

Three system timers are provided by the Intel-8253 programmable counter chip on the SBC 80/20 board. Counter 0 is currently unused, counter 1 is configured for the real-time clock (but not operational due to the interrupts), and counter 2 serves as the baud-rate generator for the console port.

DISCUSSION

The Waiver File Intelligent Terminal is used to access a data base on a larger main-frame computer. The system provides maximum flexibility by making the complex data-base management system of the main-frame computer transparent to the user.

All pertinent information regarding the Waiver File Intelligent Terminal configuration and necessary modifications has been outlined in this manual. Extensive detail on any specific device can be found by referring to the particular hardware reference manual in question, as listed in Appendix A.

TABLE 6. WAIVER FILE INTERRUPT STRUCTURE

Interrupt		
SBC 80/20 IR No.	SBC bus INT No.	Description
0	N/A	Real-time clock OIT1
1	1	Comm system RXR
1	1	Comm system TXR
2	N/A	Console RXR
3	N/A	Console TXR
4	N/A	Line printer PIB1
5	5	Carousel RXR
5	5	Carousel TXR

Blank

APPENDIX A. REFERENCE MANUAL LIST

1. SBC 80/20 Single Board Computer Hardware Reference Manual. Intel, 1977.

2. SBC 104/108/116 Combination Memory and I/O Expansion Board Hardware Reference Manual. Intel, 1978.

3. SBC 016 16K RAM Expansion Board Hardware Reference Manual. Intel, 1976.

4. Model 277 Dual Diskette Drive Installation and Maintenance Manual. PerSci, 1977.

5. Model 270 Diskette Drive Logic and Schematic Diagrams. PerSci, 1977.

6. Model 277 Diskette Drive Product Specifications. PerSci, 1977.

7. Model 1070 Intelligent Diskette Controller Users Manual. PerSci, 1978.

8. Fox-1100 Users Manual. Perkin Elmer, 1977.

9. Carousel 310 Users Manual. Perkin Elmer, 1976.

10. Operating Instructions for Model 810 Printer. Texas Instruments, 1977.

11. SBC 660 System Chassis Hardware Reference Manual. Intel, 1977.

Manufacturers' addresses:

Intel, 3065 Bowers Ave., Santa Clara CA 95051

Perkin Elmer Data Systems, Route 10 and Emery Avenue, Randolph NJ 07801

PerSci, Inc., 12210 Nebraska Ave., West Los Angeles CA 90025

T.I. Digital Systems Division, Texas Instruments Inc., P.O. Box 1444, Houston TX 77001

APPENDIX B. WAIVER FILE SYSTEM: CABLE LIST AND DIAGRAMS

TABLE B-1. CABLE LIST

Number	Description
WCA -1	Console internal cable
WCA -2	Line printer internal cable
WCA -3	Line printer external cable
WCA -4	Comm serial internal cable
WCA -5	Comm serial external cable
WCA -6	Comm parallel internal cable
WCA -7	Comm parallel external cable
WCA -8	Teleprinter internal cable
WCA -9	Floppy internal cable
WCA -10	Disk/controller cable
WCA -11	Paper-tape-reader cable
WCA -12	Comm system to modem
WCA -13	Modem to DAA convertor

Configuration notes:

1. The "W" preceding all connector and cable designators represents the Waiver File Intelligent Terminal system.

2. The "CA" represents cable.

3. SBC board connectors J1, J2, and J3 are labeled in accordance with the board slot number; i.e., AJ1, BJ1, CJ1, etc.

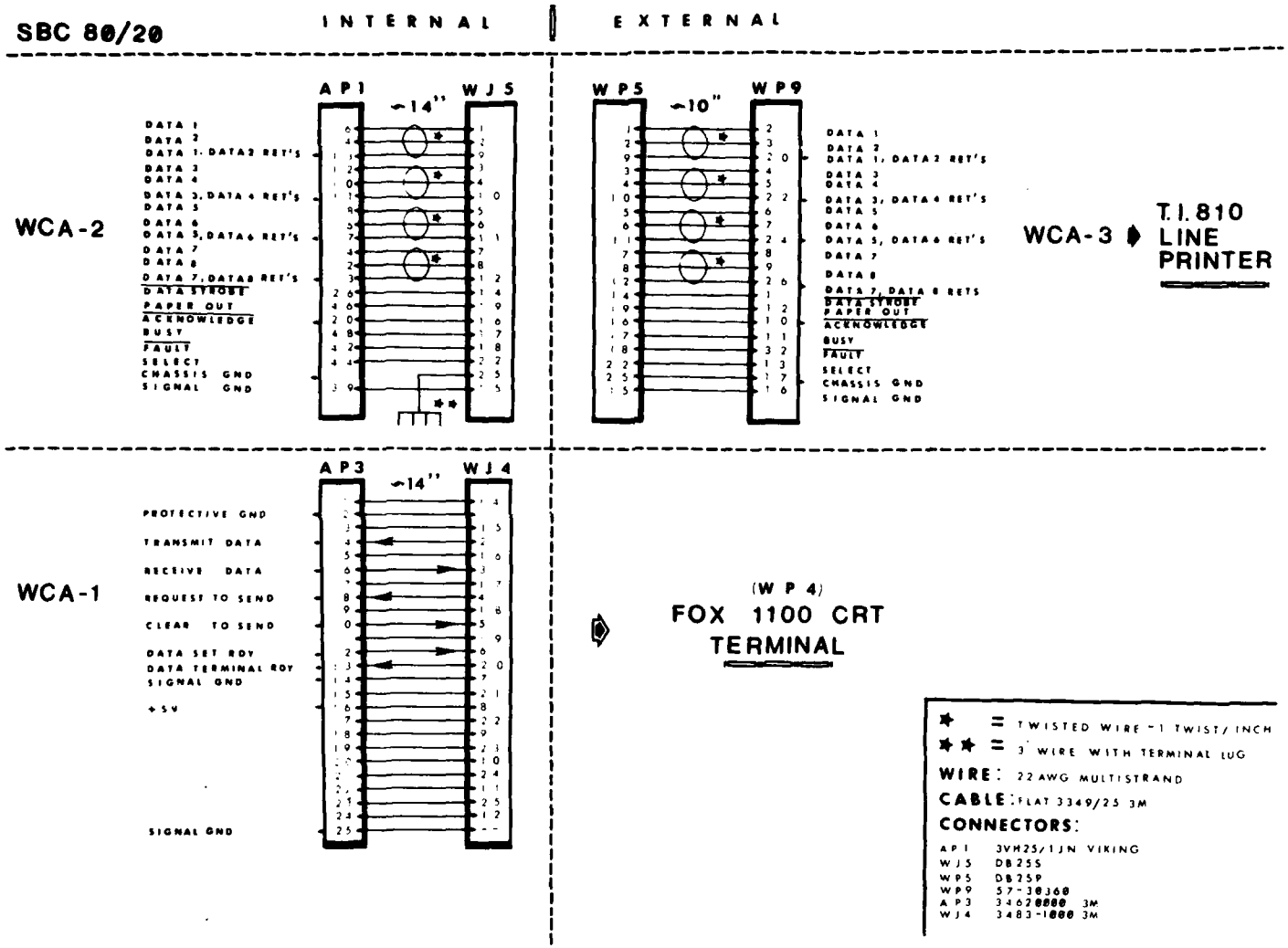

Figure B-1. Terminal and printer cable system.

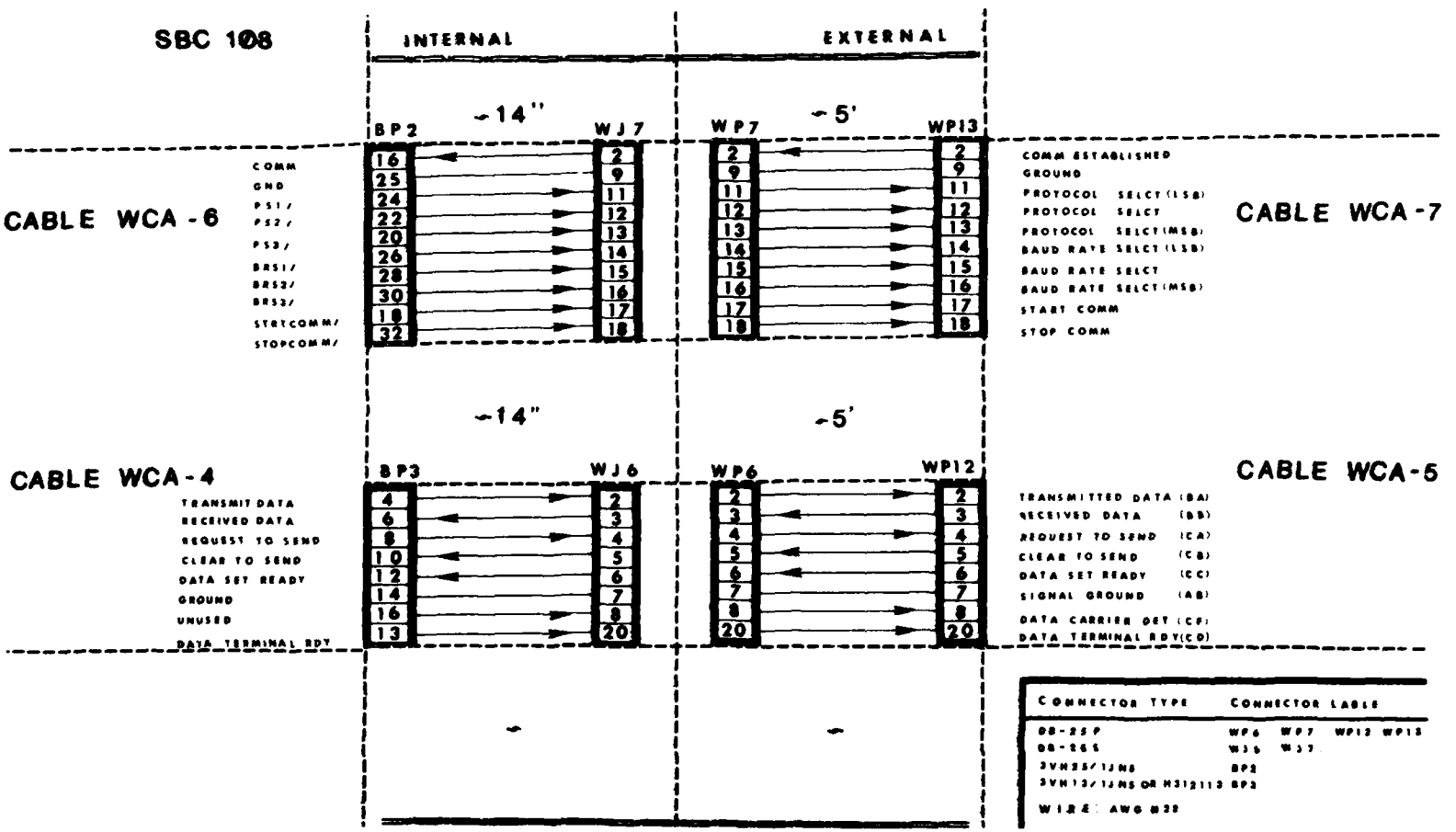

Figure B-2. Comm system control cables.

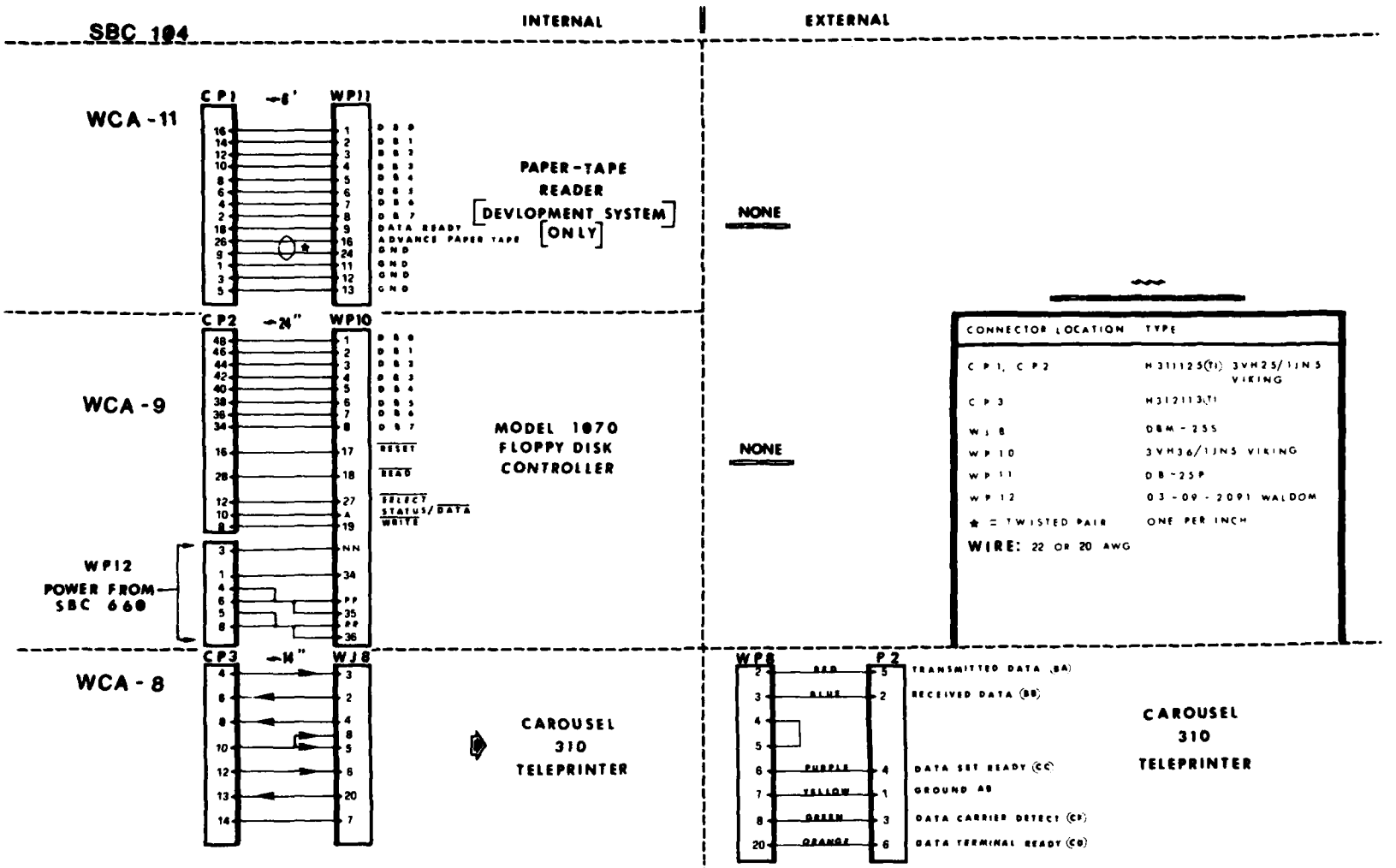

Figure B-3. Peripheral-device cables, SBC 104.


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